3 HARDWARE INTERFACE

This section presents a detailed description of the hardware interfaces for the MicroTracker LP receiver. A standard straight OSX jack receptacle is provided for the RF interface (1575.42 Mhz at a level between -130 dBW and -163 dBW). An even more compact board design can be achieved using an optional right angle OSX jack receptacle. Data input and output is through a Zero Insertion Force (ZIF) OEM interface connector or an optional 2x10 pin field connector. Pinout descriptions for each type of connector are provided in this section.

3.1 MicroTracker LP Mechanical Interface Descriptions

3.1.1 RF Input (J1). The straight RF input connector is interchangeable between an Omni Spectra (OSX) and Huber & Suhner (MCX) 50 ohm connector. Refer to Appendix H for connector specifications. Optional right angle connectors are also available. Possible mating connectors are listed in Table III-1.

Possible mating connector manufacturers are:

Macom (OSX connector)
Omni Spectra
140 Fourth Avenue
Walthham, MA 02254-9101
Telephone: (800) 366-2266

Huber & Suhner (MCX connector)
One Allen Martin Drive
P.O. Box 400
Essex, VT 05451
Telephone: (802) 878-0555

Huber & Suhner (MCX connector)
CH-9100 Herisau
Switzerland
Telephone: 071-53-41-11

Huber & Suhner (MCX Connector)
Repic Corporation
28-3 Kita Otsuka 1 Chome
Toshima-Ku/Tokyo
Japan
Telephone: 3-918-5326

3.1.2 Communications Interface (J2). The communications interface is an ELCO 6200 Series or AMP FPC 1.0 mm pitch, Zero Insertion Force (ZIF) connector. Refer to Appendix D for physical location and Appendix E for ZIF Connector and Flex Cable Specifications. An optional 2x10 pin field interface connector is also available.

Table III-1. MicroTracker LP Mating Connectors (J1)

MANUFACTURER:	PART#:	DESCRIPTION:	CABLE:
Macom-Omni Spectra	5831-5002-10	Cable Plug, Full Crimp	RG-316/U
Macom-Omni Spectra	5831-5003-10	Cable Plug, Full Crimp	RG-178/U
Macom-Omni Spectra	5837-5002-10	Cable Plug, Right Angle, Crimp Attach	RG-178/U
Macom-Omni Spectra	5807-5001-09	Cable Plug, Right Angle, Solder Attach	RG-316/U
Huber & Suhner	11 MCX-50-1-10	Cable Plug, Full Crimp	RG-178/U
Huber & Suhner	11 MCX-50-2-10c	Cable Plug, Full Crimp	RG-316/U
Huber & Suhner	16 MCX-50-1-5c	Cable Plug, Right Angle, Crimp/Solder	RG-178/U
Huber & Suhner	16 MCX-50-2-5c/111	Cable Plug, Right Angle, Crimp/Solder	RG-316/U
Huber & Suhner	16 MCX-50-3-1c	Cable Plug, Right Angle, Crimp/Solder	RG-58/U
Huber & Suhner	16 MCX-50-3-2c	Cable Plug, Right Angle, Crimp/Solder	141 semi-rigid

3 HARDWARE INTERFACE

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3.1 MicroTracker LP Mechanical Interface Descriptions

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Huber & Suhner (MCX Connector)
Repic Corporation
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Toshima-Ku/Tokyo
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Telephone: 3-918-5326

3.1.2 Communications Interface (J2). The communications interface is an ELCO 6200 Series or AMP FPC 1.0 mm pitch, Zero Insertion Force (ZIF) connector. Refer to Appendix D for physical location and Appendix E for ZIF Connector and Flex Cable Specifications. An optional 2x10 pin field interface connector is also available.

Table III-1. MicroTracker LP Mating Connectors (J1)

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Macom-Omni Spectra	5831-5003-10	Cable Plug, Full Crimp	RG-178/U
Macom-Omni Spectra	5837-5002-10	Cable Plug, Right Angle, Crimp Attach	RG-178/U
Macom-Omni Spectra	5807-5001-09	Cable Plug, Right Angle, Solder Attach	RG-316/U
Huber & Suhner	11 MCX-50-1-10	Cable Plug, Full Crimp	RG-178/U
Huber & Suhner	11 MCX-50-2-10c	Cable Plug, Full Crimp	RG-316/U
Huber & Suhner	16 MCX-50-1-5c	Cable Plug, Right Angle, Crimp/Solder	RG-178/U
Huber & Suhner	16 MCX-50-2-5c/111	Cable Plug, Right Angle, Crimp/Solder	RG-316/U
Huber & Suhner	16 MCX-50-3-1c	Cable Plug, Right Angle, Crimp/Solder	RG-58/U
Huber & Suhner	16 MCX-50-3-2c	Cable Plug, Right Angle, Crimp/Solder	141 semi-rigid

3.1.3 Board Dimensions For The MicroTracker LP. Refer to the Appendix D Mechanical Reference Drawing (TU00-D200).

3.1.4 Flex Cable Manufacturers. Possible mating flex cable manufacturers are:

AXON Cable Inc.
390 E. Higgins Road, Suite 101
Elk Grove Village, IL 60007
(708) 806-6629/FAX: (708) 806-6639

W. L. Gore & Associates Inc.
4747 East Beautiful Lane
Phoenix, AZ 85076
1-800-228-3024

Bando Desen Co., Ltd.
Office 4/20-16 Hizaore
Asaka, Saitama, Japan
0484-61-0561

Parlx Corp.
145 Milk Street
Methuen, MA 01844
(508) 685-4341

Fujikura Ltd.
1400 - 100 Galleria Parkway NW
Atlanta, GA 30339
(404) 955-3596

Spectra Systems (Distributor)
600 N. Pine Island Road, Suite 175
Plantation, FL 33324
(305) 475-0070

AXON Cable, France
Paris France
33-26-81-70-00
Request Export Department

3.1.5 ZIF Connector Suppliers. ZIF connector suppliers are:

ELCO, U.S.A.
3250 Keller Street, Unit One
Santa Clara, CA 95054
(408) 496-1861

T.T.I., Inc.
4033 E. Belknap
Ft. Worth, TX 76111
(817) 831-9985
(National distributor for ELCO, U.S.A.)

ELCO Germany
ELCO Elektronik GmbH
Benjamin Fox Strasse 1
5240 Betzdorf, West Germany
49-2741-2990

ELCO International, K. K.
1794 Nippa-Cho, Kohoku-Ku
Yokohama 223, Japan
81-45-545-1499

ELCO International
1-800-653-3526
Maintains stock in U.S.A. for Rockwell GPS receiver customers.

3.1.6 2x10 Pin Field Connector Supplier. The 2x10 pin field connector is a Molex 70287 Series dual row, straight pin field header (Molex part number 10-96-7205). The connector supplier is:

Molex, Inc.
2222 Wellington Ct.
Lisle, IL 60532
(708) 969-4550

3.2 MicroTracker LP Electrical Interface Descriptions

3.2.1 RF Interface.

3.2.1.1 Impedance. The input impedance at the RF connector is 50 ohms with a VSWR of 2:1 or better.

3.2.1.2 Center Frequency Input. The input center frequency is 1575.42 MHz.

3.2.1.3 Signal Level Input. The operational input range is -163 to -130 dBW (with operational satellite signals).

3.2.1.4 Noise Figure Input. The composite noise figure of a preamplifier, cable, and GPS receiver must be less than 5.0 dB for operation with minimum

guaranteed GPS satellite signal levels. A composite noise figure of 8 dB may be used for operation with typical GPS satellite signal levels. To determine this composite noise figure, a typical noise figure of 4.0 dB is used for the GPS receiver, measured at the RF input port at L1 with a 10 MHz bandwidth. The methodology to compute composite noise figure is described in Section 6.

3.2.1.5 Input Burnout Protection. The maximum input power level is -10 dBW at the RF port (at L1 with a 10 MHz bandwidth).

3.2.1.6 Delay. The delay, or line length, between the antenna and J1 RF connector is not important. The Microtracker LP will compute a navigation solution at the phase-center of the antenna.

3.2.1.7 **Antenna.** The antenna is required to be right-hand circular polarized, exhibiting a gain of not less than -3 dBIc above a 10 degree elevation.

3.2.2 OEM Interface. A pinout description for the ZIF interface connector is provided in Table III-2. Figure 3-1 diagrams the pin 1 reference location for this connector. A pinout description for the 2x10 pin field connector is provided in Table III-3. Figure 3-2 diagrams the pin 1 reference location for this connector.

The following paragraphs describe the basic functions allocated to the various pins on the ZIF and the 2x10 pin field interface connectors. These functions are divided into three groups: DC input signals, serial communication signals, and control and timing signals.

3.2.2.1 DC Input Signals.

3.2.2.1.1 Power Input (ZIF: J2-21 and 26) (2x10 Pin Field: J2-2)

"PWRIN" Input is the main power input to the MicroTracker LP. Regulated DC power requirements are shown in Table I-3.

Primary DC input voltage must be 4.75 volts or greater for proper operation. For the ZIF connector, both input pins should be connected to 5 volts.

3.2.2.1.2 Preamp Power Input (ZIF: J2-23) (2x10 Pin Field: J2-1)

Voltage = +12V DC (max)
Current = 100 mA (max)

The OEM may optionally supply power to a preamplifier using the antenna cable center conductor. Maximum voltage is 12V DC and the current must not exceed 100 mA.

WARNING: DO NOT APPLY POWER TO A PASSIVE ANTENNA OR DAMAGE TO THE RECEIVER WILL OCCUR.

3.2.2.1.3 VBATT1 Battery Input (ZIF: J2-15) (2x10 Pin Field: J2-10)

"Keep Alive" power input to SRAM and the RTC (+5V to +3V DC). This is intended to provide the MicroTracker LP with a "hot start" capability by maintaining position, time, and ephemeris data in SRAM when prime power has been removed from the receiver.

VBATT1 supply voltage can vary from a minimum of +2.50V DC to a maximum of +5.25V DC. "Keep-Alive" power dissipation will vary depending on the chosen VBATT1 supply voltage. Table I-3 shows typical power dissipation for VBATT1 supply voltages of +5V DC and +3V DC.

3.2.2.1.4 VBATT2 Battery Input (ZIF: J2-20) (2x10 Pin Field: J2-5)

"Keep Alive" power input to the RTC only (+5V to +3V DC). This is intended to provide the MicroTracker LP with a "warm start" capability by maintaining an accurate time source and using position and satellite almanac data stored in EEPROM after prime power has been removed from the receiver.

VBATT2 supply voltage can vary from a minimum of +2.50V DC to a maximum of +5.25V DC. "Keep-Alive" power dissipation will vary depending on the chosen VBATT2 supply voltage. Typical power dissipation for VBATT2 supply voltages of +5V DC and +3V DC is shown in both Table I-3 and Table III-4.

Table III-2. MicroTracker LP ZIF OEM Interface Connector Pinout

PIN:	NAME:	DESCRIPTION:
1	DTR2	DATA TERMINAL READY FALSE PORT 2 (NO CONNECT)
2	SDIN2	SERIAL PORT 2 DATA INPUT
3	INV2	SERIAL PORT 2 POLARITY INVERT
4	SDO2	SERIAL PORT 2 DATA OUTPUT
5	MR	MASTER RESET LOW
6	GND	GROUND
7	TMARK	TIME MARK PULSE
8	GND	GROUND
9	N/C	NO CONNECT
10	N/C	NO CONNECT
11	GPIO4	GENERAL PURPOSE I/O 4; NMEA SELECT (+5V = NMEA, GND = BINARY)
12	GPIO3	GENERAL PURPOSE I/O 3; RESERVED (NO CONNECT)
13	GPIO2	GENERAL PURPOSE I/O 2; RESERVED (NO CONNECT)
14	GPIO1	GENERAL PURPOSE I/O 1; BAUD RATE SELECT (+5V = 9600 BAUD, GND = 4800 BAUD)
15	VBATT1	BACKUP BATTERY #1 (SRAM & RTC)
16	DTR1	DATA TERMINAL READY FALSE PORT 1
17	SDIN1	SERIAL PORT 1 DATA INPUT
18	INV1	SERIAL PORT 1 POLARITY INVERT
19	SDO1	SERIAL PORT 1 DATA OUTPUT
20	VBATT2	BACKUP BATTERY #2 (RTC ONLY)
21	PWRIN	+5V DC POWER
22	GND	GROUND
23	PREAMP	PREAMP POWER
24	GND	GROUND
25	N/C	NO CONNECT
26	PWRIN	+5V DC POWER

NOTE: N/C and reserved pins required to be left open (unconnected).

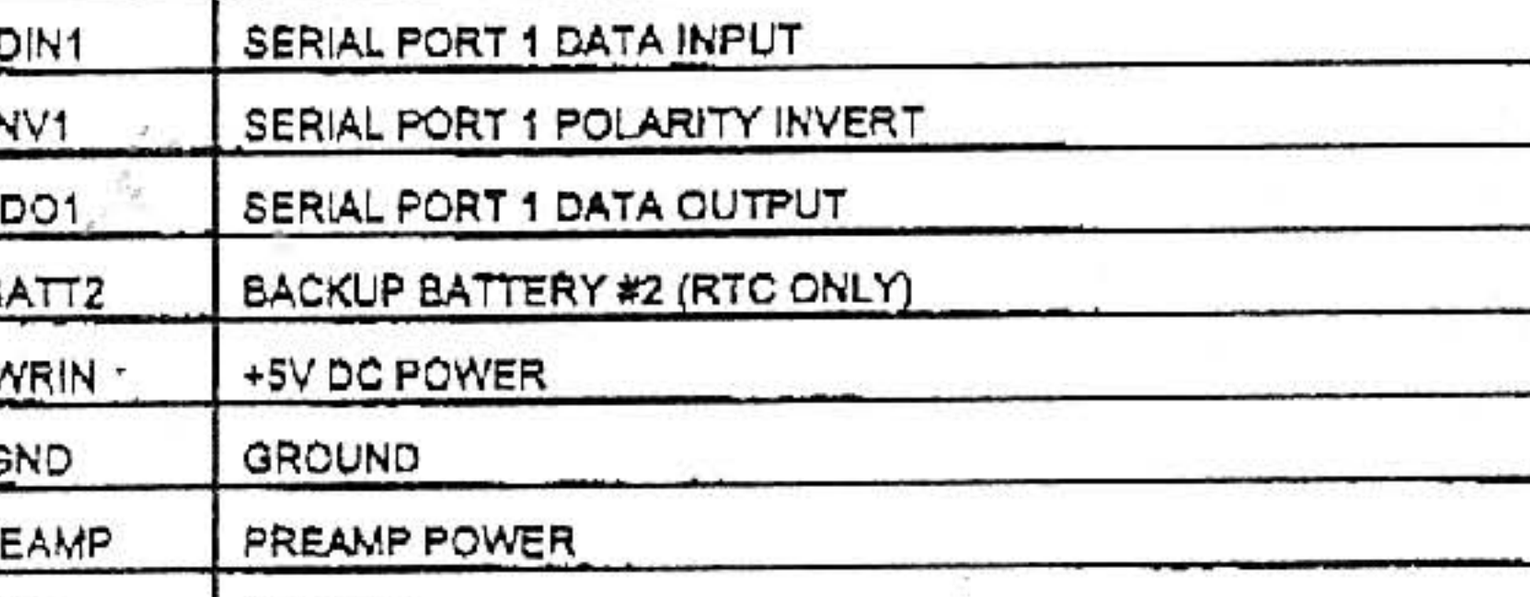

Figure 3-1. ZIF Connector (J2) Pin 1 Reference Location

Table III-3. MicroTracker LP Standard 2X10 Pin Field OEM Interface Connector Pinout

PIN:	NAME:	DESCRIPTION:
1	PREAMP	PREAMP POWER
2	PWRIN	+5V DC POWER
3	GND	GROUND
4	GPIO4	GENERAL PURPOSE I/O 4; NMEA SELECT (+5V = NMEA, GND = BINARY)
5	VBATT2	BACKUP BATTERY #2 (RTC ONLY)
6	SDO1	SERIAL DATA PORT 1 DATA OUTPUT
7	TMARK	TIME MARK PULSE 1 PPS
8	DTR1	DATA TERMINAL READY FALSE PORT 1
9	SDIN1	SERIAL PORT 1 DATA INPUT
10	VBATT1	BACKUP BATTERY #1 (SRAM & RTC)
11	GND	GROUND
12	GPIO3	GENERAL PURPOSE I/O 3; RESERVED (NO CONNECT)
13	MR	MASTER RESET LOW
14	GND	GROUND
15	GPIO2	GENERAL PURPOSE I/O 2; RESERVED (NO CONNECT)
16	SDO2	SERIAL PORT 2 DATA OUTPUT
17	GND	GROUND
18	SDIN2	SERIAL PORT 2 DATA INPUT
19	GND	GROUND
20	GPIO1	GENERAL PURPOSE I/O 1; BAUD RATE SELECT (+5V = 9600 BAUD, GND = 4800 BAUD)

NOTE: Reserved pins required to be left open (unconnected).

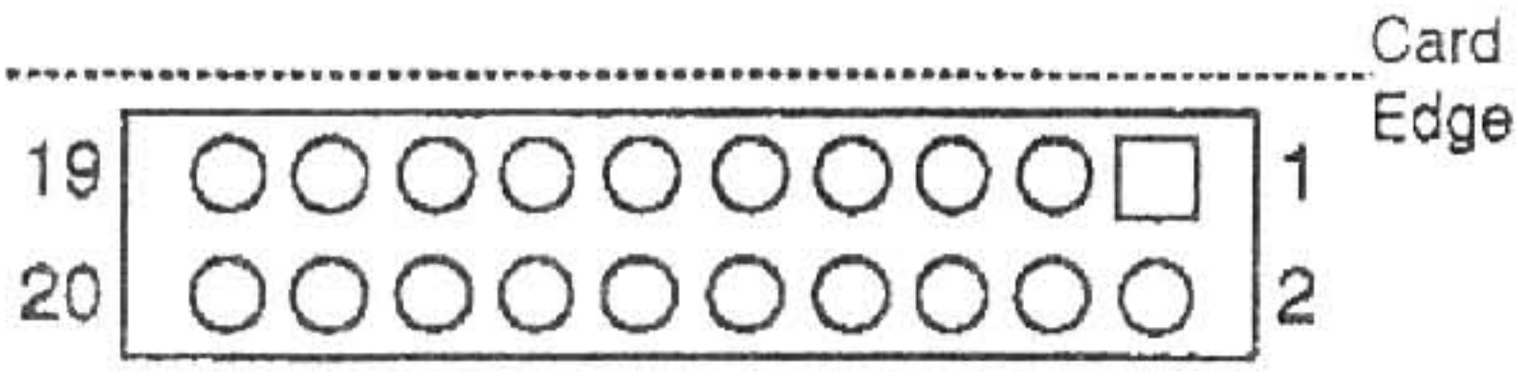

Figure 3-2. 2x10 Pin Field Connector (J2) Pin 1 Reference Location

Table III-4. MicroTracker LP Operational Modes Summary

INPUT SIGNALS:	OPERATIONAL MODES							
	OFF	OPERATE	"KEEP-ALIVE"	"KEEP-ALIVE"	"KEEP-ALIVE"	"KEEP-ALIVE" (RTC Only)	"KEEP-ALIVE" (RTC Only)	POWER MANAGE-MENT
PWRIN Voltage	0V or GND	5V	5V	0V or GND	0V or GND	0V or GND	0V or GND	5V
PWRIN Current	–	167 mA (835 mW)	0.360 mA (1.8 mW)	–	–	–	–	(see Table I-4)
VBATT1 Voltage	0V or GND	N/A	N/A (Note 1)	5V	3V	N/A	N/A	N/A
VBATT1 Current	–	–	–	0.030 mA (0.15 mW)	0.016 mA (0.048 mW)	–	–	–
VBATT2 Voltage	0V or GND	N/A	N/A	N/A	N/A	5V	3V	N/A
VBATT2 Current	–	–	–	–	–	<200 nA (<1 µW)	<100 nA (<0.3 µW)	–
Master Reset Signal	Floating or GND	High	GND	Floating or GND	Floating or GND	Floating or GND	Floating or GND	High
Serial I/O	N/A	N/A	Un-driven or HI-Z (Note 2)	Un-driven or HI-Z (Note 2)	Un-driven or HI-Z (Note 2)	Un-driven or HI-Z (Note 2)	Un-driven or HI-Z (Note 2)	N/A

Note 1: "Keep-Alive" voltage for SRAM and RTC is provided by the PWRIN supply.

Note 2: Serial data input signals for both auxiliary and host ports should be de-energized or maintained at high impedance (HI-Z) by the OEM application for the lowest power dissipation in "Keep-Alive" mode.

3.2.2.1.5 Ground (ZIF: J2-6, 8, 22, and 24) (2x10 Pin Field: J2-3, 11, 14, 17, and 19)
DC ground for the board. All grounds are tied together through the MicroTracker LP's printed wiring board (PWB) ground plane and should all be grounded externally to the MicroTracker LP.

3.2.2.2 Serial Communication Signals. The signals described in this section and in section 3.2.2.3 must be applied according to the requirements of Table III-5.

3.2.2.2.1 Host Port Serial Data Input/Output (ZIF: J2-17 and 19) (2x10 Pin Field: J2-6 and 9)
The host port consists of a full-duplex asynchronous serial data interface. Both binary and NMEA initialization and configuration data messages are transmitted and recieved across this port. The OEM application system will be required to provide any Line Driver/Line Receiver (LD/LR) circuitry to extend the range of the interface. Port Idle is nominally a logical high (+5V DC).

3.2.2.2.2 Host Port Data Terminal Ready (DTR1) (ZIF: J2-16) (2x10 Pin Field: J2-8)
Peak data rate control for serial messages transmitted across the host port is provided on this pin. An active high inhibits serial data output on the host port. An active low enables serial data output. This control signal is pulled low by default on the MicroTracker LP's PWB through a 51K Ohm resistor to ground.

3.2.2.2.3 Host Port Data Polarity Invert (INV1) (ZIF: J2-18) (2x10 Pin Field: N/A)
When asserted, the active polarity of the host port's serial data input and output signals is inverted. An

Table III-5. MicroTracker LP Digital Signal Requirements

SYMBOL:	PARAMETER:	LIMITS:	UNITS:
VIH (min)	Minimum High-Level Input Voltage	0.7 x PWRIN	volts
VIH (max)	Maximum High-Level Input Voltage	PWRIN	volts
VIL (min)	Minimum Low-Level Input Voltage	-0.3	volts
VIL (max)	Maximum Low-Level Input Voltage	0.3 x PWRIN	volts
VOH (min)	Minimum High-Level Output Voltage	0.8 x PWRIN	volts
VOH (max)	Maximum High-Level Output Voltage	PWRIN	volts
VOL (min)	Minimum Low-Level Output Voltage	0	volts
VOL (max)	Maximum Low-Level Output Voltage	0.2 x PWRIN	volts
tr, tf	Input Rise and Fall Time	50	nanoseconds
C out	Maximum Output Load Capacitance	25	picofarads

active high inverts the serial data polarity (Port Idle becomes a logical "low" signal level). This control signal is pulled low by default on the MicroTracker LP's PWB through a 51K Ohm resistor to ground.

3.2.2.2.4 Auxiliary Port Serial Data Input/Output

(ZIF: J2-2 and 4)
(2x10 Pin Field: J2-16 and 18)

The auxiliary port consists of a second full-duplex asynchronous serial data interface. While the hardware supports both input and output capability, the current software supports only input of RTCM DGPS correction data.

The OEM application system will be required to provide any LD/LR circuitry to extend the range of the interface. Port Idle is nominally a logical high (+5V DC). The digital signal requirements for the serial data interface are summarized in Table III-5.

3.2.2.2.5 Auxiliary Port Data Terminal Ready (DTR2)

(ZIF: J2-1)
(2x10 Pin Field: N/A)

This capability is not available since the auxiliary port is used for data input only.

3.2.2.2.6 Auxiliary Port Data Polarity Invert (INV2)

(ZIF: J2-3)
(2x10 Pin Field: N/A)

When asserted, the active polarity of the auxiliary port's serial data input and output signals is inverted. An active high inverts the serial data polarity (Port Idle becomes a logical "low" signal level). This control signal is pulled low by default on the MicroTracker LP's PWB through a 51K Ohm resistor to ground.

3.2.2.3 Control and Timing Signals

3.2.2.3.1 Master Reset (MR)

(ZIF: J2-5)
(2x10 Pin Field: J2-13)

This signal provides the OEM with control of the MicroTracker LP's Operate mode without removing prime input power from the receiver. This signal can also be used to generate a system reset to the receiver. When the MR is pulled to ground by the OEM, the receiver will enter the "Keep-Alive" mode as long as the MR is maintained at ground level. The receiver will generate a system reset and return to Operate mode when MR is removed from ground level and is asserted high.

NOTE: The MR must be held at ground level for a minimum of 150 nanoseconds to assure generation of a hardware reset to the system. The MicroTracker LP's power consumption in "Keep-Alive" mode is summarized in both Table I-3 and Table III-4.

3.2.2.3.2 Time Mark Pulse (ZIF: J2-7)
(2x10 Pin Field: J2-7)

The Time Mark output provides a one pulse-per-second (pps) signal to the OEM application processor. This pulse represents the instant in time when the navigation solution is valid. The precision of the Time Mark output is ±1 microsecond (µsec), exlusive of the effects of Selective Availability (SA).

This pulse is provided for synchronization with the Time Mark output message (binary Message 103; refer to Section 4) which contains the local estimate of GPS time and position. The Time Mark Pulse width is 20 µsec and the polarity is positive going. The navigation solution that is provided subsequent to the pulse contains solution data that is valid at the rising edge of the Time Mark Pulse. The Time Mark Pulse logic level is +5V DC HCMOS.

3.2.2.3.3 Baud Rate Select (GPIO1) (ZIF: J2-14)
(2x10 Pin Field: J2-20)

The data communication rate over the host serial I/O port is selectable. When this signal is asserted "high" the baud rate and data protocol are: 9600 Baud RX/TX, odd parity, and 1 stop bit.

When this signal is pulled "low," the baud rate and data protocol are: 4800 baud RX/TX, no parity, and 1 stop bit (NMEA standard communication parameters).

This control signal is pulled "high" by default through a 5.1K Ohm resistor located on the MicroTracker LP's PWB. The standard host port configuration of 9600 baud RX/TX, odd parity, and 1 stop bit is therefore enabled by default upon power-up of the receiver.

Regardless of the selected baud rate, the serial communication protocol is 1 start bit, 8 data bits (least significant bit transmitted first), parity bit, and 1 stop bit. For more detail, refer to Section 4 of this manual.

3.2.2.3.4 General Purpose I/O 2 (GPIO 2)
(ZIF: J2-13)
(2x10 Pin Field: J2-15)

This signal is reserved for future use and should be left as a no-connect by the OEM application.

3.2.2.3.5 General Purpose I/O 3 (GPIO 3)
(ZIF: J2-12)
(2x10 Pin Field: J2-12)

This signal is reserved for future use and should be left as a no-connect by the OEM application.

3.2.2.3.6 NMEA Protocol Select (GPIO 4)
(ZIF: J2-11)
(2x10 Pin Field: J2-4)

The MicroTracker LP has two hardware selectable message protocols that may be used to communicate over the host serial I/O port. When this signal is pulled "low," the default input/output message protocol is the binary format messages defined in Section 4 of this manual.

When this signal is pulled "high," the receiver will output NMEA initialization and configuration data messages and will accept NMEA query and proprietary input message over the host port as defined in Section 5 of this manual.

The Rockwell binary format message protocol is enabled by default upon power-up of the receiver since this control signal is pulled "low" through an internal resistor within MicroTracker LP's Digital Signal Processor. To select the NMEA format message protocol, this signal must be pulled "high" by the OEM application through a 10K Ohm or less pull-up resistor tied to PWRIN (+5V DC).

3.2.2.3.7 Reserved (ZIF: J2-9, 10, and 25)
(2x10 Pin Field: N/A)

This signal is reserved for future use and should be left as a no-connect by the OEM application.

3.2.3 Power Modes. The MicroTracker LP has four power modes: Off, Operate, Power Management, and "Keep-Alive." Table III-4 summarizes the signal conditions for the various MicroTracker LP operational modes.

The Off mode implies that the receiver is completely de-energized. The Operate mode implies that the receiver is completely energized. The Power Management mode provides a way in which the user may lower the receiver's average power consumption by reducing the frequency of navigational updates. The "Keep-Alive" mode implies that minimal power is being dissipated to preserve time and critical data.

- **Off mode.** The receiver is completely de-energized including all DC supply input signals, serial data input signals, and control input signals.
- **Operate mode.** The receiver enters its Operate power mode when PWRIN supply voltage is applied. The PWRIN supply voltage must be greater than +4.75V DC. The MR control signal must be floating or at a CMOS "high" logic level.
- **Power Management mode.** In this mode, PWRIN supply voltage is applied within its proper operating range. Depending on the navigation data update rate selected by the OEM, the receiver will operate with lower average power consumption. See Table I-4 for DC power consumption by the receiver in its Power Management mode.
- **"Keep-Alive" mode.** From Operate mode, the MicroTracker LP will enter its "Keep-Alive" power mode by either removing PWRIN voltage or by asserting the MR control signal. The difference in these two methods is which power source (PWRIN, VBATT1, or VBATT2) supplies the "Keep-Alive" power and the amount of power dissipated by the receiver while in the "Keep-Alive" mode.

In the first method, when PWRIN is removed from the MicroTracker LP, VBATT1 and/or VBATT2 must be present and stable for correct battery switch-over operation. If VBATT1 is present, both the SRAM and RTC will be energized. If VBATT1 is not present and VBATT2 is present, only the RTC will be energized. To achieve the lowest power dissipation possible when in "Keep-Alive" mode, the OEM must ensure that PWRIN voltage is de-energized (0V DC) and that the serial communication signals, and control and timing signals are de-energized (not driven to a CMOS high level) or floating. See Table III-4 for power dissipation values in the "Keep-Alive" mode.

In the second method, asserting the MR control signal will also put the receiver in a "Keep-Alive" mode in the following three instances:

1) If PWRIN is not de-energized (5V DC) when the MR control signal is asserted (active low), PWRIN will be the power source for maintaining the SRAM and RTC.
2) If the OEM de-energizes PWRIN (0V DC) when asserting the MR control signal, VBATT1 will be the power source for maintaining the SRAM and RTC.
3) If the OEM de-energizes PWRIN (0V DC) when asserting the MR control signal and VBATT1 is not present, VBATT2 will be the power source for maintaining only the RTC.

Power dissipation for the above three instances are defined in Table III-4.

Violation of the specified operating voltages will result in erratic receiver operation. +4.5(+0/-0.2)V DC is the voltage thresold level at which the receiver's power supervisory circuit places the receiver's microprocessor in reset; PWRIN will continue to supply power to the receiver. No damage will occur to the MicroTracker LP if PWRIN dwells in this uncertainty region, but power dissipation will be affected. Also, critical SRAM data and RTC time keeping may become corrupted, affecting TTFF when the receiver is returned to normal operating conditions.

CAUTION: During the OFF or "Keep-Alive" modes, it is recommended that the serial communication signals, and the control and timing signals are de-energized (not driven to a CMOS high level) or floated. If the host system does apply power to these signals while the MicroTracker LP is turned OFF, no damage to the receiver will occur since these signals are protected by series resistors.

3.2.4 Power Input. Regulated DC power is required according to that shown in Table I-3.

3.2.5 Power-Up Sequencing. The power-up sequence for the MicroTracker LP is the same for both the OFF mode and the "Keep-Alive" mode. Primary DC power, as specified in Table I-3, is applied to the PWRIN pin of the MicroTracker LP interface by the host system. If the MR pin on the interface is asserted high when DC power is applied, the receiver will begin normal operation after 200 milliseconds. If the MR pin is asserted low (or ground), the receiver will remain off or enter the "Keep-Alive" mode depending on whether the receiver was previously operating (refer to Table III-4).